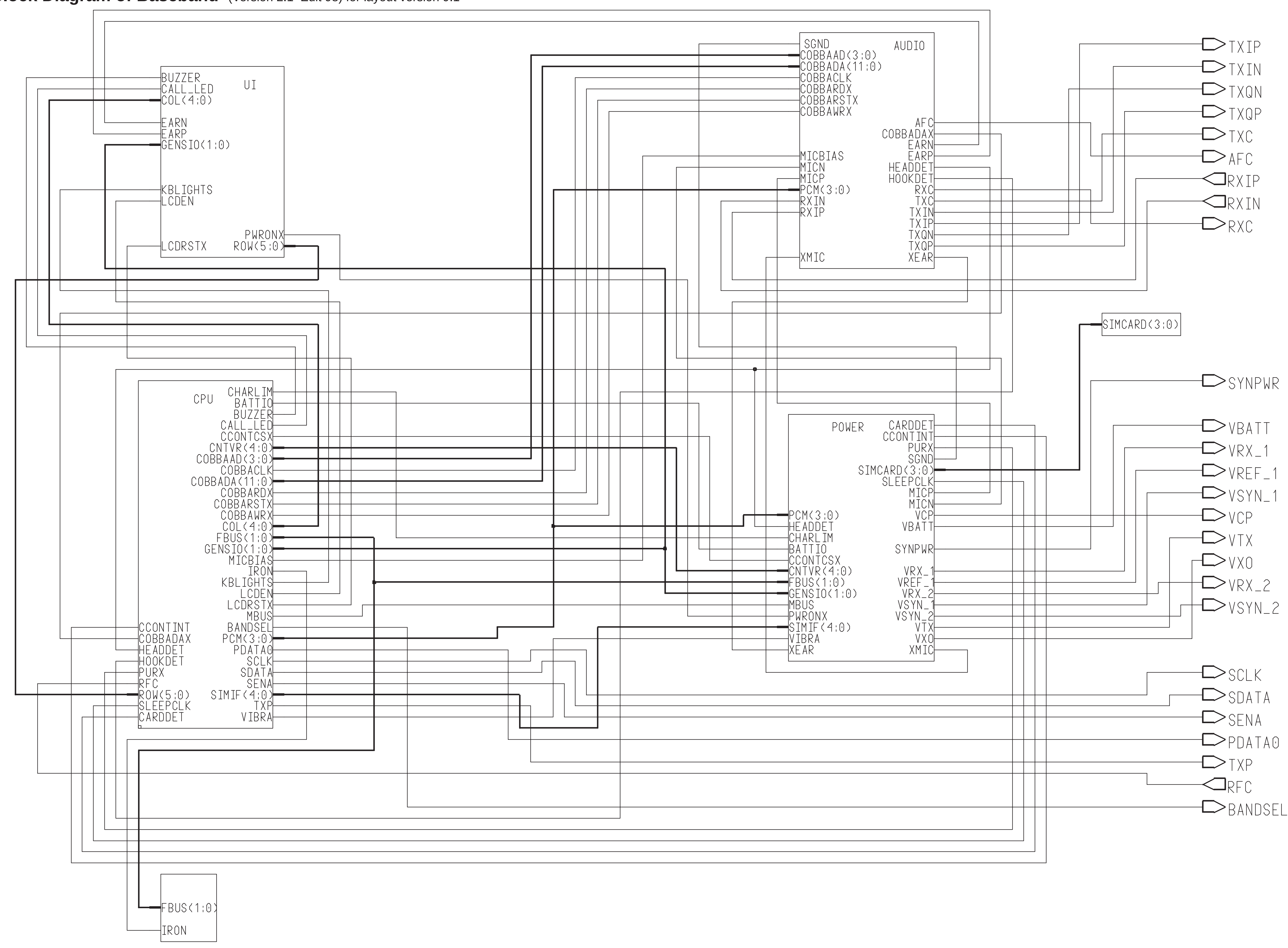
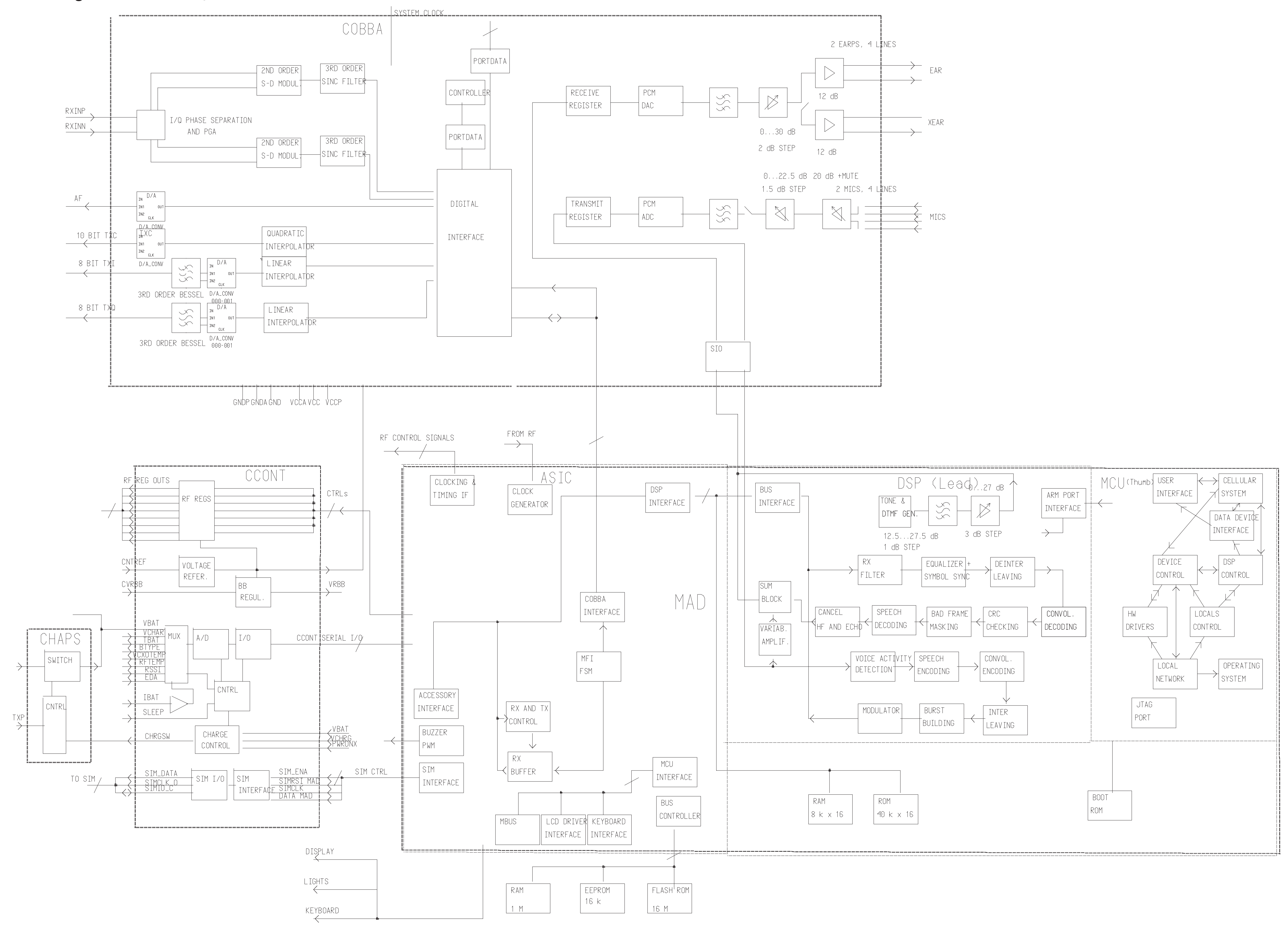
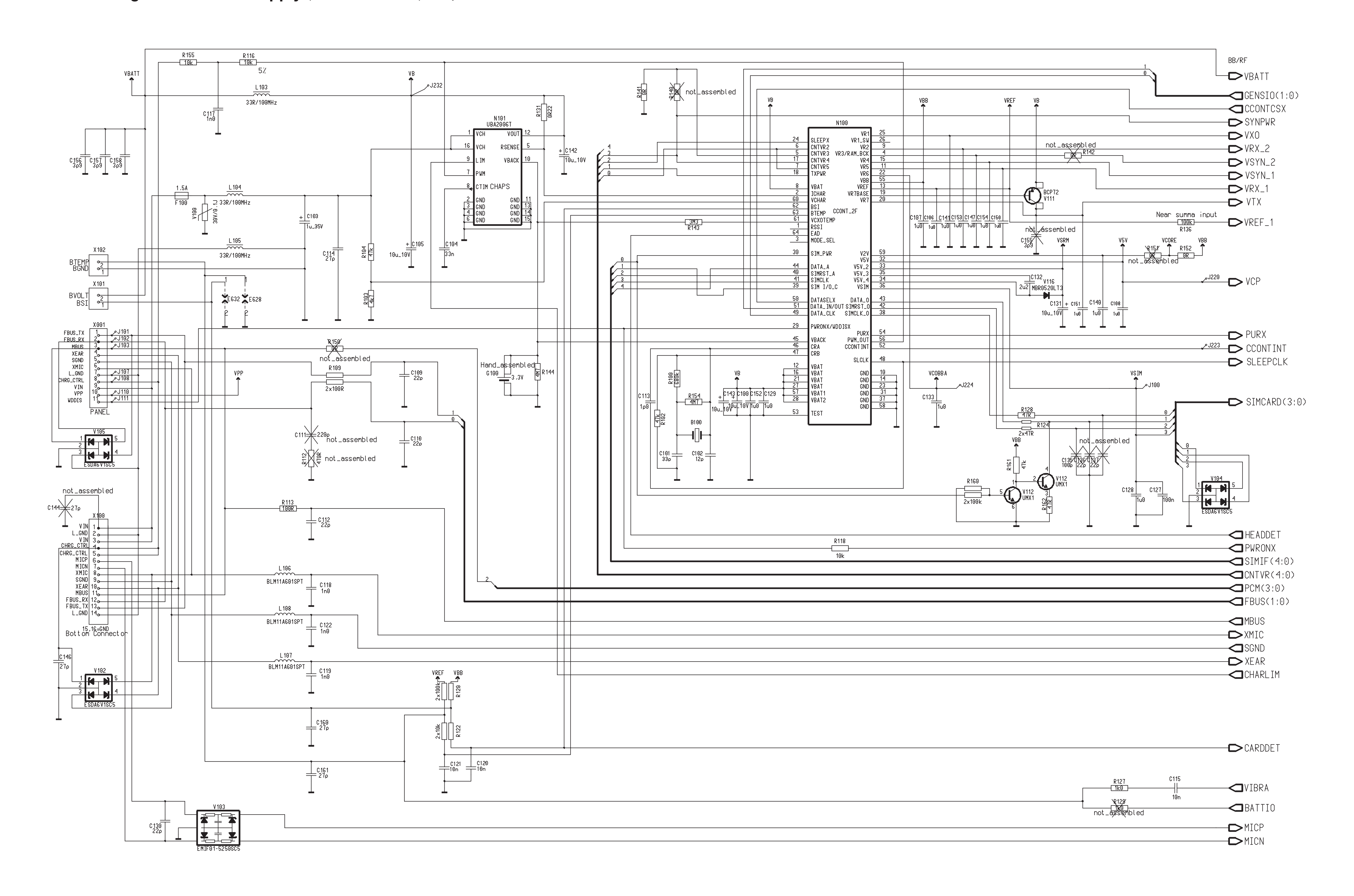
Block Diagram of Baseband (Version 2.1 Edit 98) for layout version 9.1



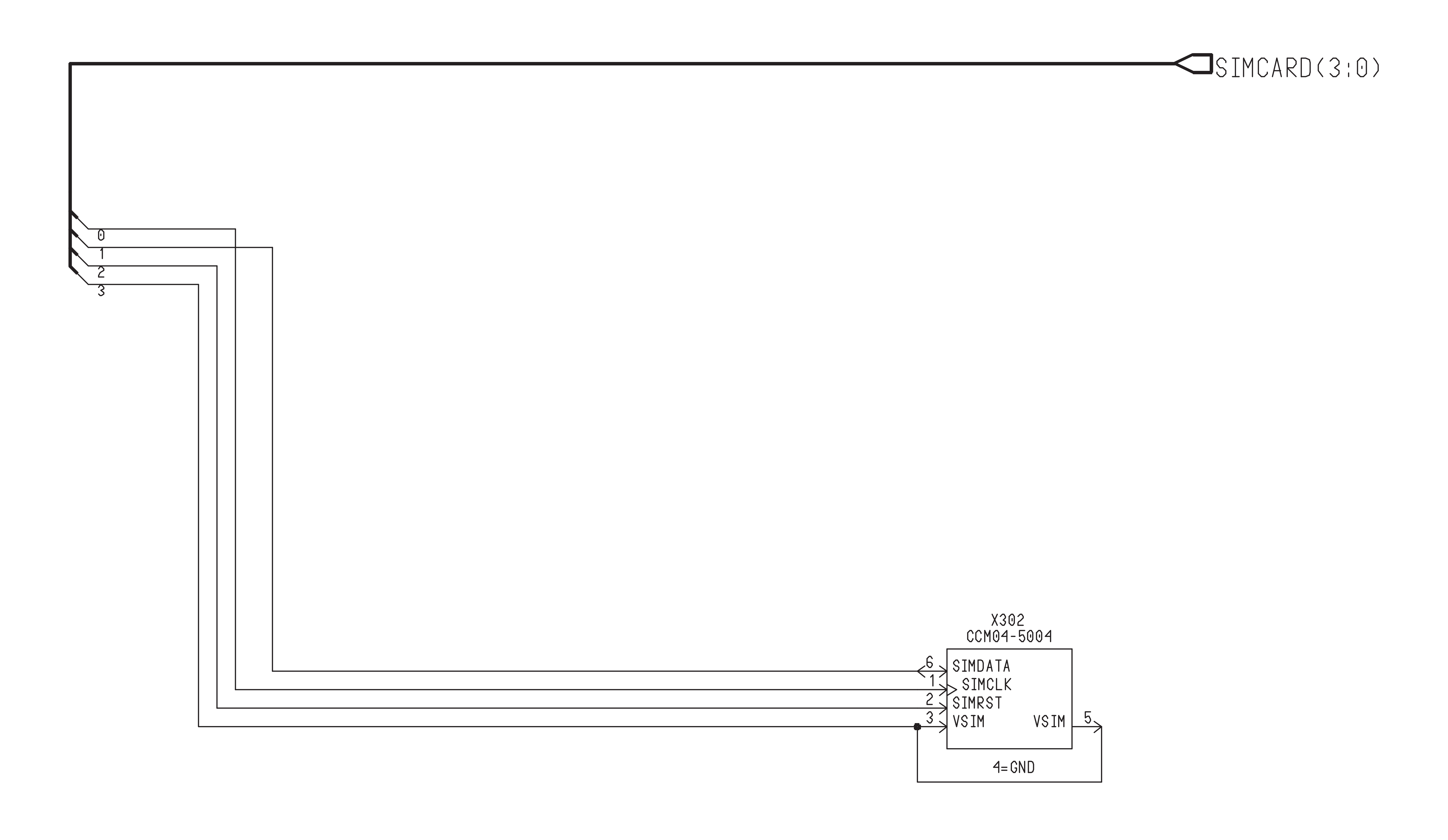
Block Diagram of COBBA, CCONT and MAD



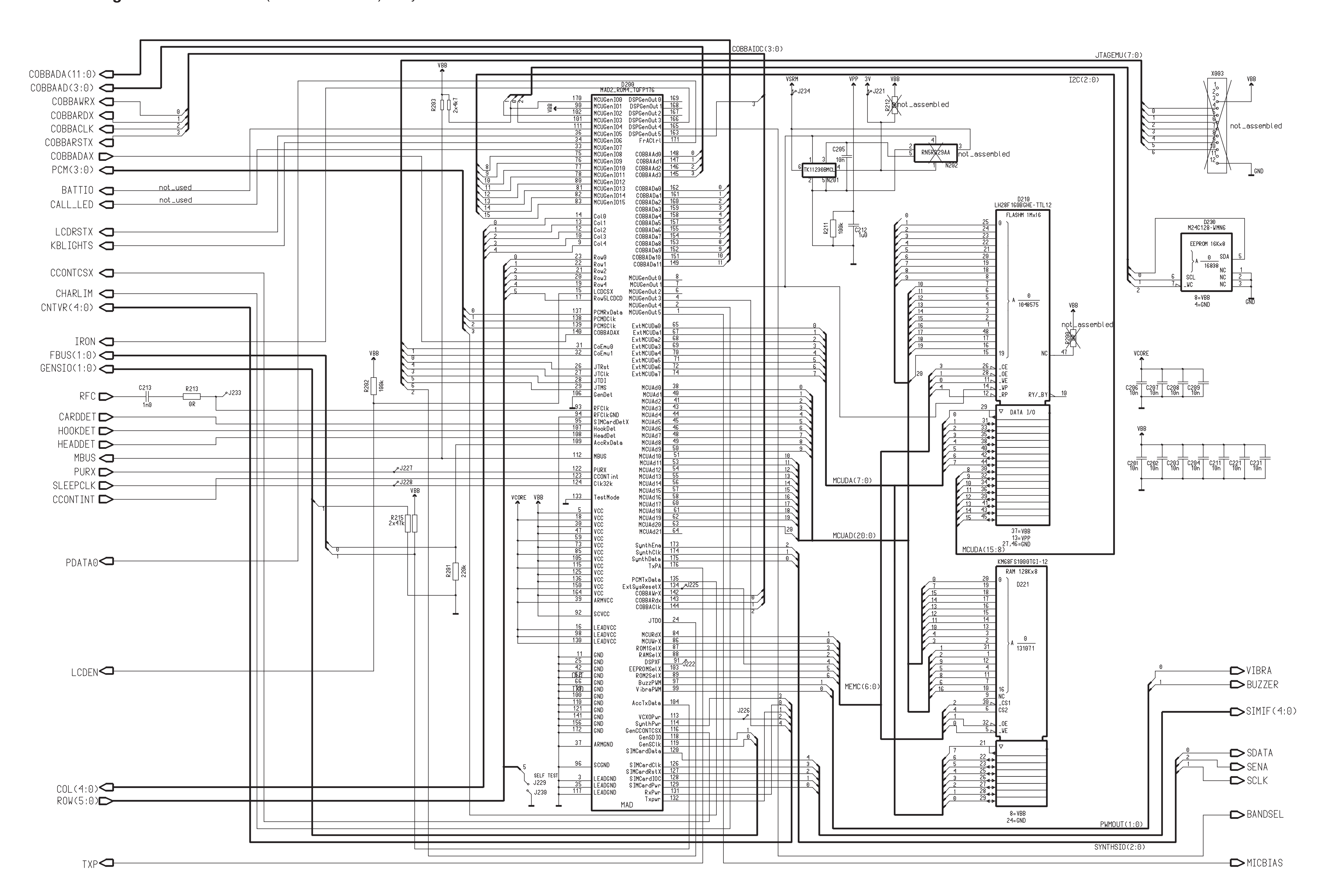
Circuit Diagram of Power Supply (Version 2.2 Edit 295) for layout version 10.3



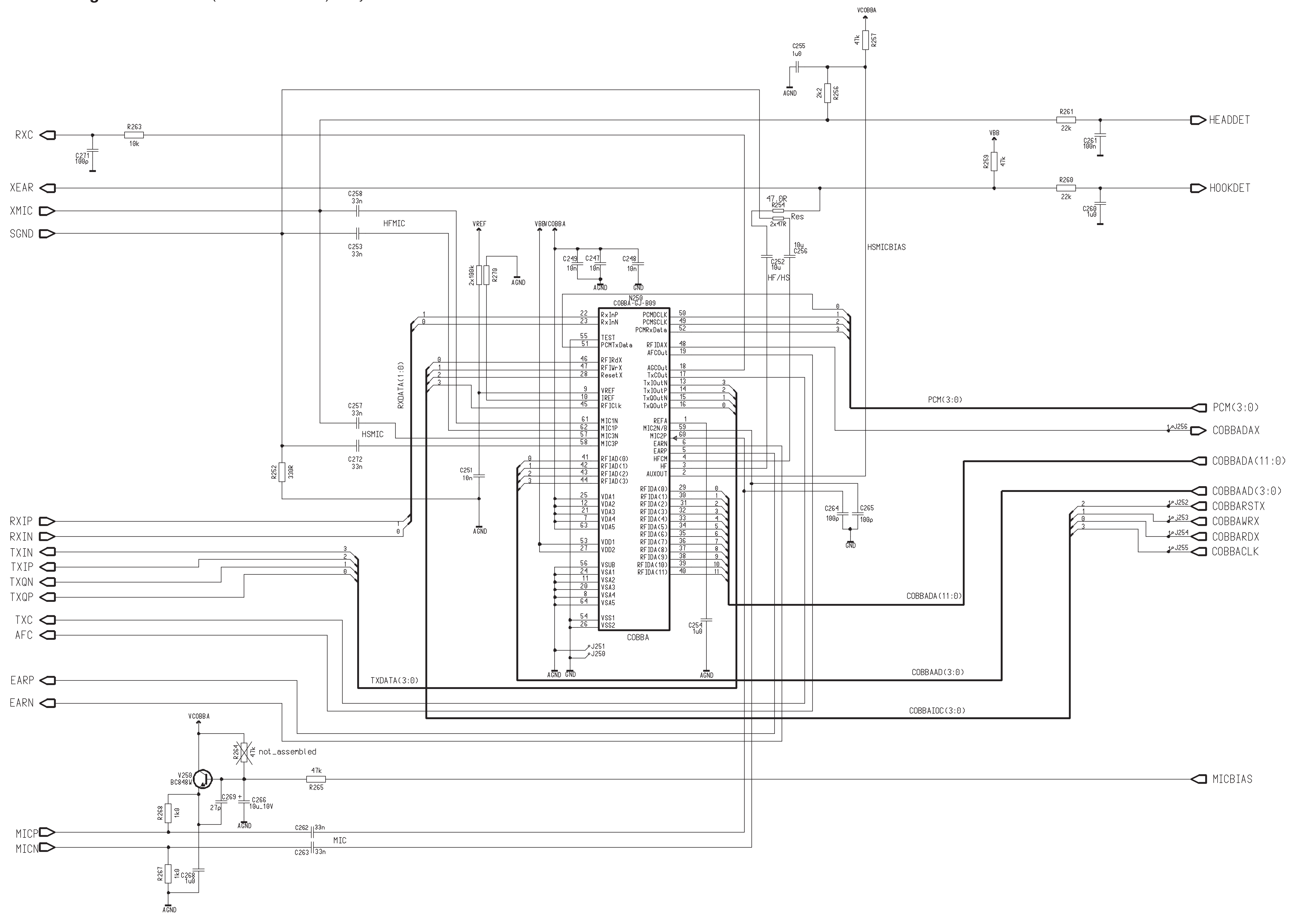
Circuit Diagram of SIM Connector (Version 2.2 Edit 97) for layout version 10.3



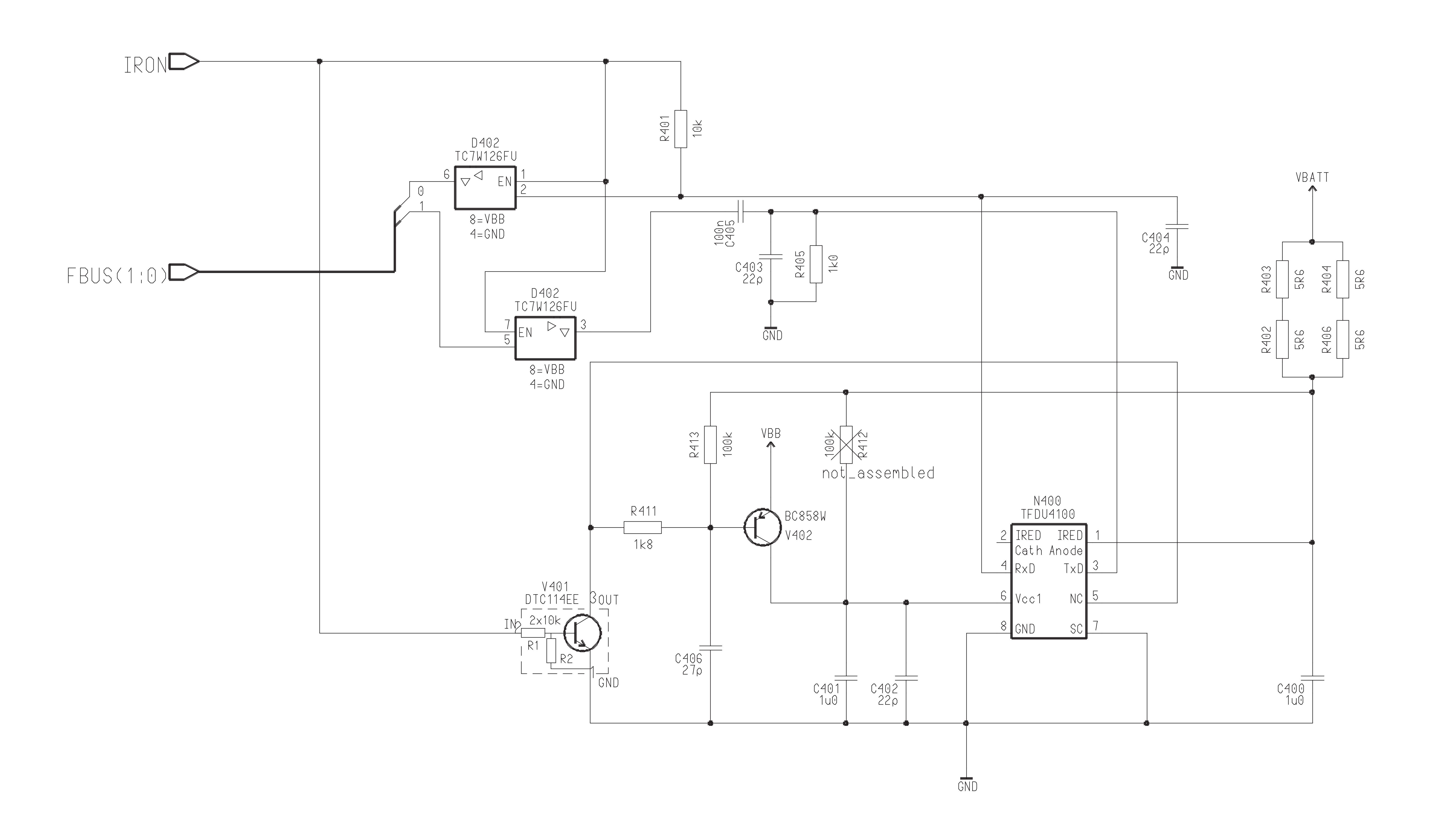
Circuit Diagram of CPU Block (Version 2.2 Edit 200) for layout version 10.3



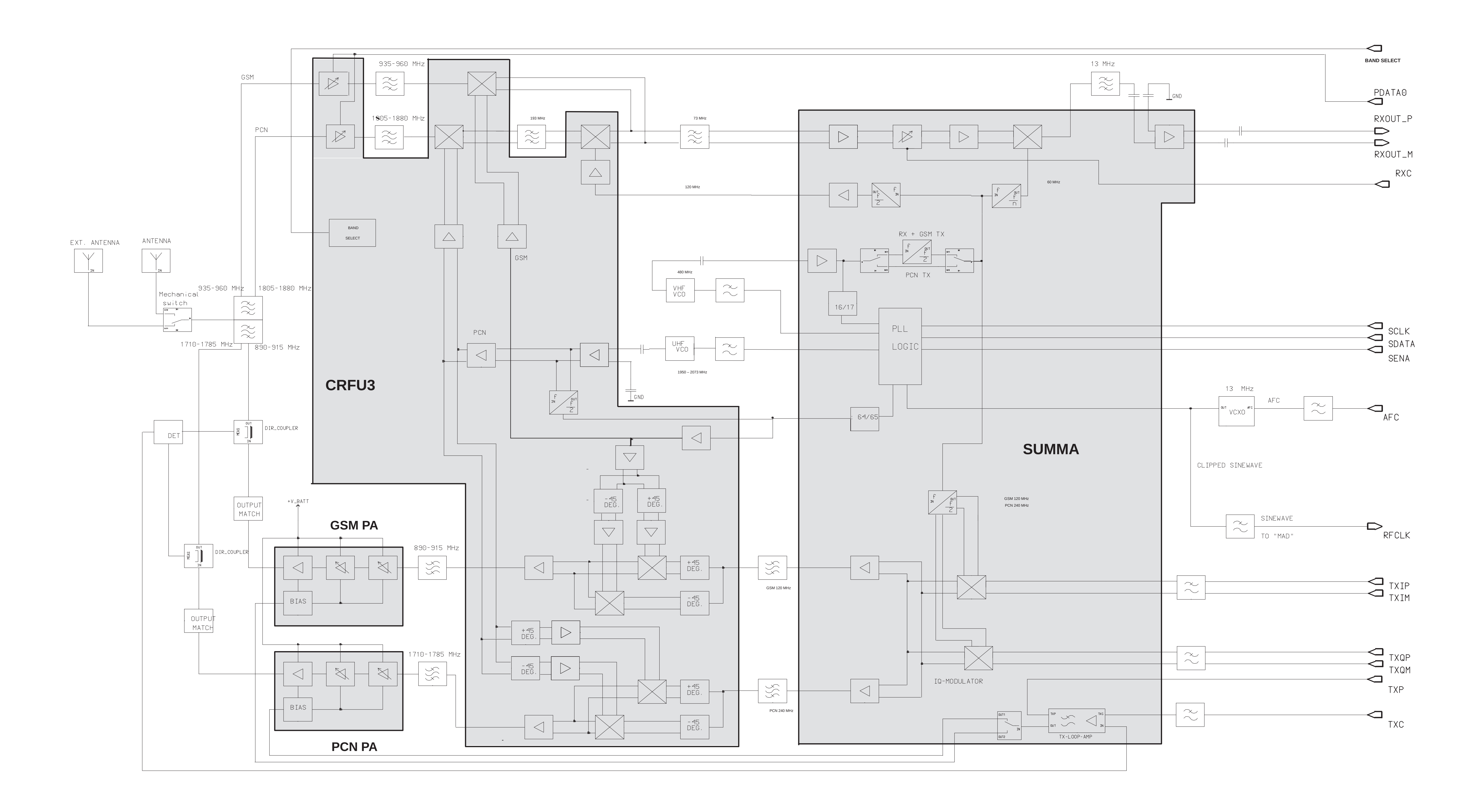
Circuit Diagram of Audio (Version 2.2 Edit 155) for layout version 10.3



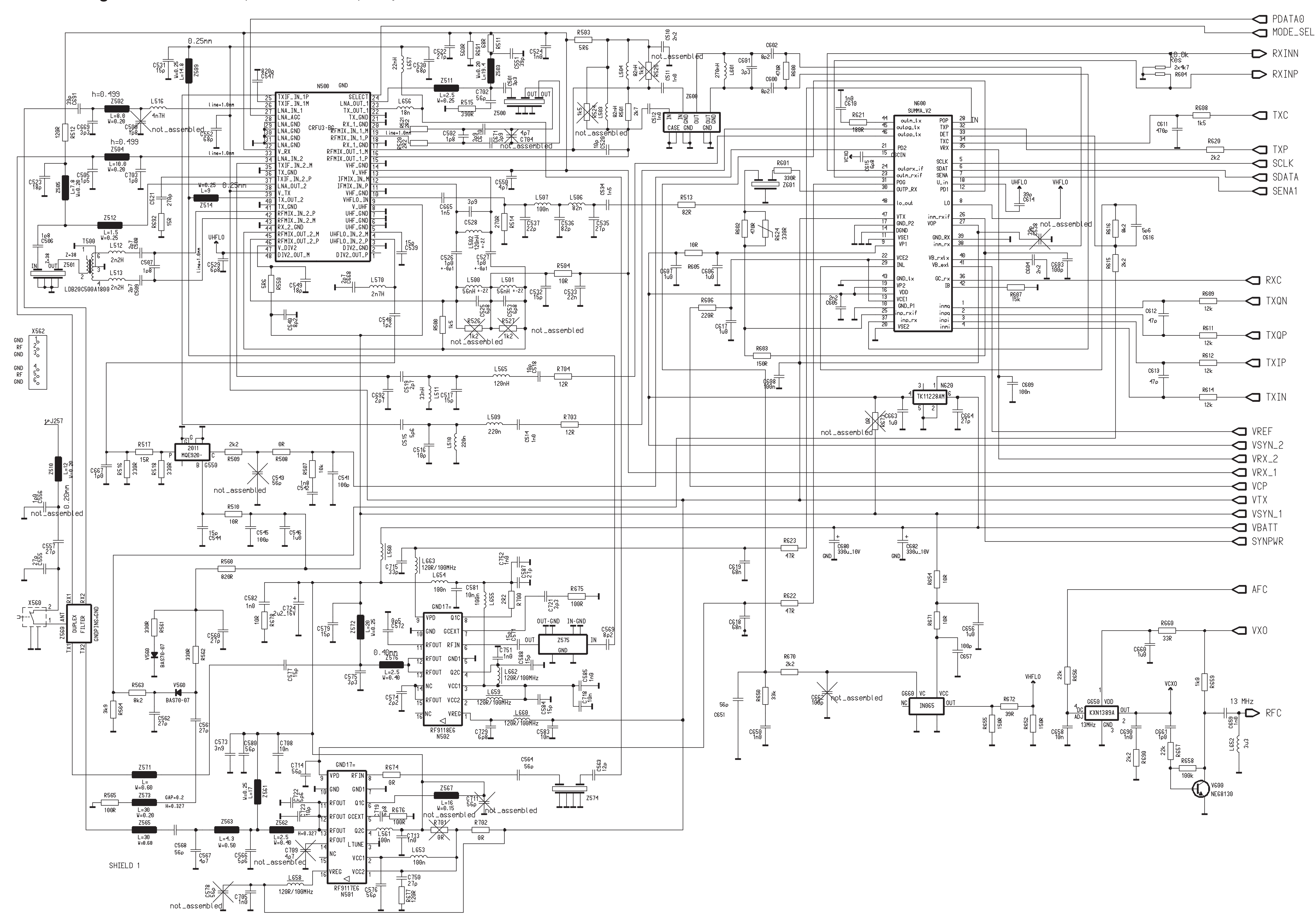
Circuit Diagram of IR Module (Version 2.2 Edit 126) for layout version 10.3



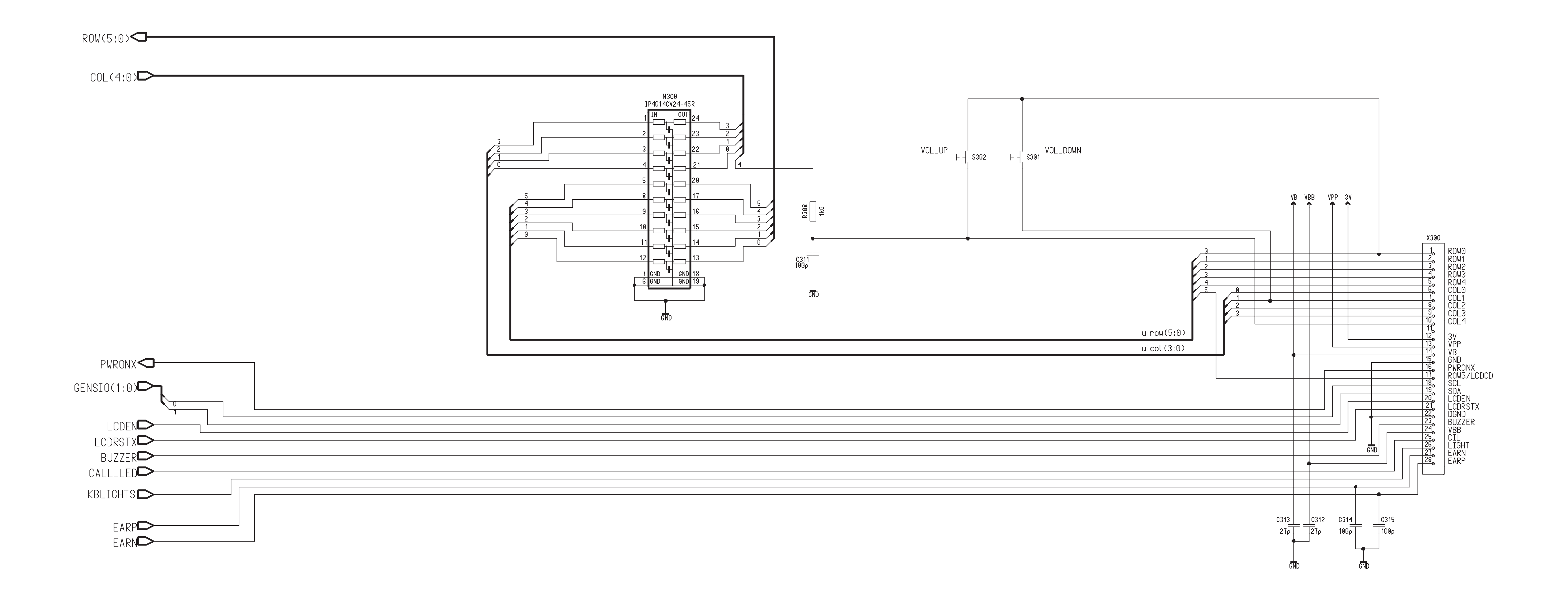
RF Block Diagram



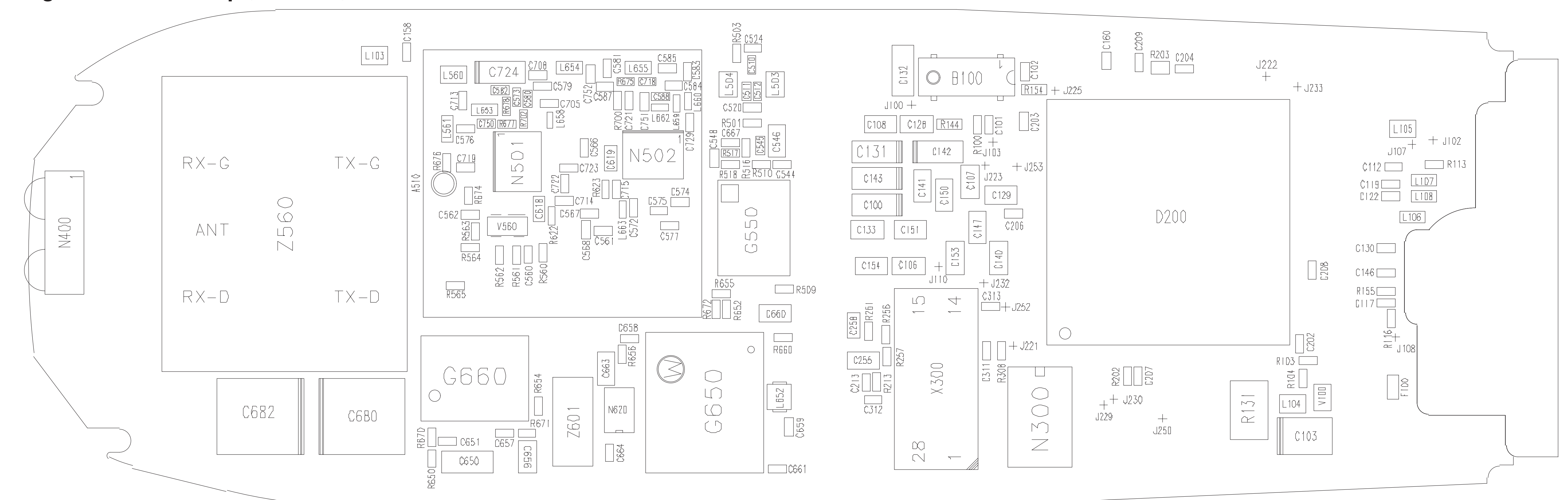
Circuit Diagram of RF Block (Version 2.2 Edit 382) for layout version 10.3



Circuit Diagram of UIF (Version 2.2 Edit 124) for layout version 10.3



Layout Diagram of UG3 – Top (Version 10.3)



Layout Diagram of UG3 – Bottom (Version 10.3)

X100
D210
D221
N100
N250
N101
Z600
N500
N600
Z500
Z574
X101
X102
X302
X560
S301
S302
J257

testpoint ref	name	condition	dc–level	ac–level
J101	FBUS_TX	active state	pulsed DC (0V72.8V)	
J104	CCONTCSX (CCONT chip select)	active state	pulse active 0V, non–active 2.8V	
J108	CHRG_CTRL	charger connected	pulsed DC (0V/2.8V)	
J220	V5V	active state	nominal 5.0V (min 4.8V, max 5.2V)	
J223	CCONTINT (charger, RTC interrupt)	interrupt	pulse active 2.8V, non–active 0V	
J225	EXTSYSRESETX	power on	reset state 0V, normal state 2.8V	
J226	VCXOPWR	power on	active state 2.8V, non–active 0V	
J227	PURX (power on reset)	power up/down	reset state 0V, normal state 2.8V	
J228	SLEEPCLK (32kHz clock)	power on	pulsed DC (0V/2.8V)	
J235	ROM1SELX	active state	pulse active 0V, non–active 2.8V	
J251	AGND	pcb ground	0V	
J256	COBBADAX	active state	pulse active 0V, non–active 2.8V	
J500	Control voltage for UHF VCO module G600	channel 60 channel 1 channel 124	2.25 +/– 0.25 V > 0.8 V < 3.7 V	
J504	Control voltage for VHF VCO circuit		typ. 2.0 –2.2 V min 0.5 / max 4.0 V	
J508	VSYN_2 (regulated supply for PLLS)		2.8 V min 2.7 / max 2.85 V	
J534&J536	13 MHz IF output to N250	–95 dBm @ X540 (ext. RF connector) RXC at level of full calibrated gain	typ ca. 1.0 – 1.1 V pulsed min. 0.7 / max. 1.4 V	typ. 50 mVpp balanced voltage at 13 MHz
J538	13 MHz output from Z620 to N620	–95 dBm @ X540 (ext. RF connector) RXC at level of full calibrated gain	typ. ca. 1.5 V pulsed	typ. ca 600 uVrms
J542	VHF VCO output (232 MHz)		–	typ. 400 mVpp. > 100 mVpp required
J554	TXC (TX power control voltage)		@level 19 typ. ca. 0.6 V pulse @level 5 typ ca. 1.8 V pulse	
J556	TXP (TX enable)		2.8 V logic level pulse, (max. 0.8 V ”0” / min 2.0 V ”1”)	
J558	TXQP (other half of balanced Q–signal)		0.8 V pulsed	400 mVpp
J560	TXIP (other half of balanced I–signal)		0.8 V pulsed	400 mVpp